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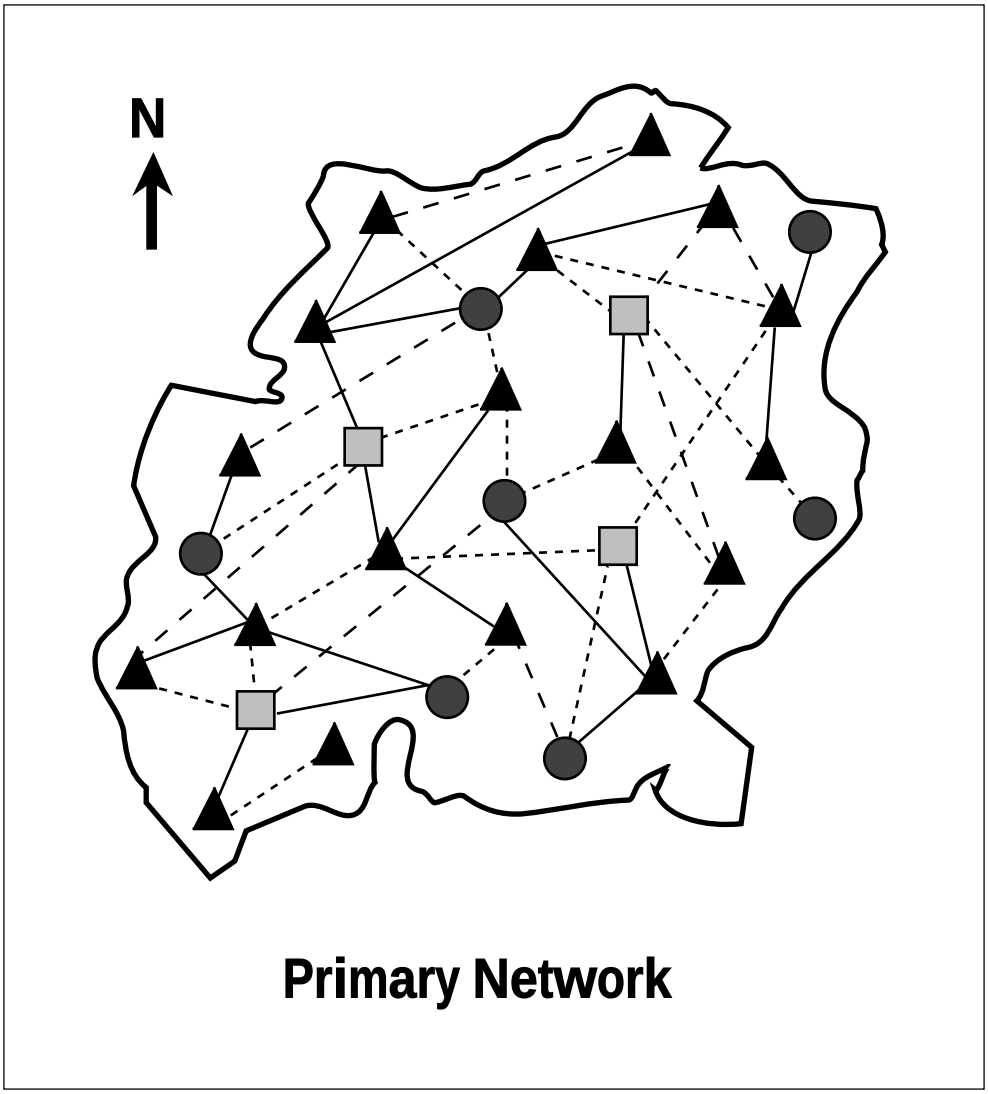
Synchronizing Telecommunications Networks:

Fundamentals of Synchronization Planning

Application Note 1264-3



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I. Introduction

In recent years, the importance of synchronization has increased due to the extensive digitization of telecommunications networks and to the introduction of SDH and SONET technologies. These events have placed more demands on synchronization planning, performance, and operation. All networks require stringent synchronization planning to meet acceptable performance levels. Improper synchronization planning or the lack of planning can cause severe performance problems. Improper planning can result in excessive slips, long periods of network downtime, elusive maintenance problems, or high transmission error rates. A proper synchronization plan, which optimizes the performance, must be made for the entire digital network.

The role of synchronization planning is to determine the distribution of synchronization in a network and to select the level of clocks and facilities to be used to time the network. This involves the selection and location of master clock(s) for a network, the distribution of primary and secondary timing throughout a network, and an analysis of the network to ensure that acceptable performance levels are achieved.

The first three sections of this application note provide the synchronization background for planning. Section II describes the major methods used for synchronization. Basic planning concepts are presented in Section III and planning requirements are covered in Section IV.

Synchronization planning of carrier networks is the topic of Section V. A brief discussion of the performance of carrier networks is given. The use, selection, and location of primary reference sources are covered. Interoffice and intraoffice timing distribution are explained next, with a focus on the selection of BITS clocks and distribution of timing from them. Section V also discusses the monitoring and verification of network synchronization performance, followed by a brief description of the special synchronization needs and concerns of SDH and SONET.

Since private network synchronization planning is very different than carrier network planning, it is considered separately. Section VI covers private networks. Private network performance is discussed, since it plays a major role in private network synchronization planning. The sources of synchronization, interoffice timing, and intraoffice timing are subsequently covered. Special concerns with dynamically changing synchronization plans and SDH/SONET conclude the section on private networks.

References are cited throughout this application note and included in brackets [ ]. A complete listing of references is on page 24.

Additional supporting material on synchronization performance, clock performance, and clock functionality is given in [1].

II. Synchronization Architecture

Major Methods For Synchronization

There are several major methods used to synchronize digital networks: plesiochronous operation, hierarchical source-receiver operation, mutual synchronization, pulse stuffing, and pointers. These are defined below.

Plesiochronous

Each node receives a reference from a different independent timing source (Figure 1). Tolerable slip rates are maintained due to tight timing accuracy of either side of the connection. Standards place a boundary on the accuracy of clocks used to time plesiochronous connections. In networks that use plesiochronous operation, controlling clocks must maintain long-term frequency accuracy to 1×10^{-11}. This mode of operation is typical for connections across administration boundaries.

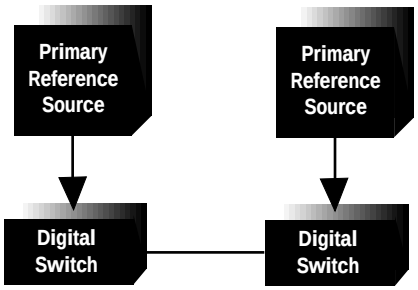

Figure 1. Plesiochronous operation.

Hierarchical Source-Receiver

A primary reference source at a master node generates a reference clock that is shared and distributed (Figure 2). The source node sends its reference to receiver nodes. The reference clock is hierarchically distributed throughout the network. The two major components of this network are the receiver clocks used to regenerate the reference clock and the digital paths used to transmit the clock through the network.

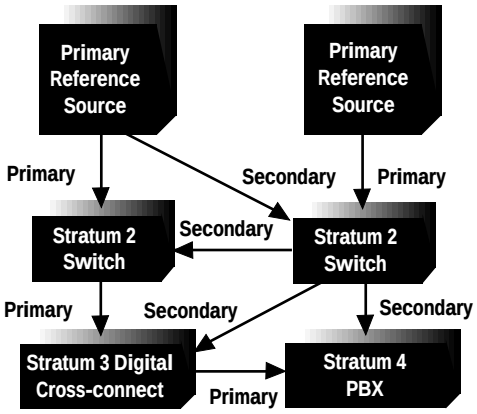

Figure 2. Hierarchical source-receiver operation.

Mutual Synchronization

In mutual synchronization, clocking information is shared by all nodes in the network (Figure 3). Each clock sends and receives a timing reference to (from) all other clocks in the network. Network timing is determined by each clock by averaging the synchronization signals it receives from all other clocks in the network. This operation can theoretically provide identical timing signals to each node, but in actual application with imperfect clocks and imperfect transmission of timing information, the timing fluctuates as it hunts for a common frequency.

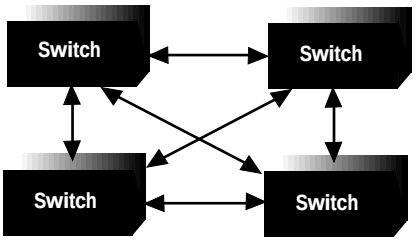

Figure 3. Mutual synchronization operation.

Pulse Stuffing

This method is used to transmit asynchronous bit streams above the DS1/E1 level, with the exception of SDH and SONET transport. The bit streams to be multiplexed are each stuffed with additional dummy pulses. This raises their rates to that of an independent local clock. The outgoing rate of the multiplexer is higher than the sum of the incoming rates. The dummy pulses carry no information and are coded for identification. At the receiving terminal, the dummy pulses are removed. The resulting gaps in the pulse stream are then removed, restoring the original bit stream. In this manner, a DS1 or E1 signal can be transmitted with the original timing information intact. The effect of pulse stuffing is to add small amounts of jitter to the DS1 or E1 signal.

Pointers

This method is used by SDH and SONET to transmit payloads that are not necessarily synchronous to the SDH/SONET clock. Pointers are used to indicate the beginning of a frame in the payload. Frequency differences between SDH/SONET network elements or between the payload and the SDH/SONET equipment are accommodated by adjusting the pointer value (Figure 4). Therefore, the payload does not need to be synchronized to the SDH/SONET equipment. SDH/SONET equipment is usually synchronized so that the number of pointer adjustments are kept to a minimum. This is desirable since each pointer adjustment will cause jitter and wander on the payload.

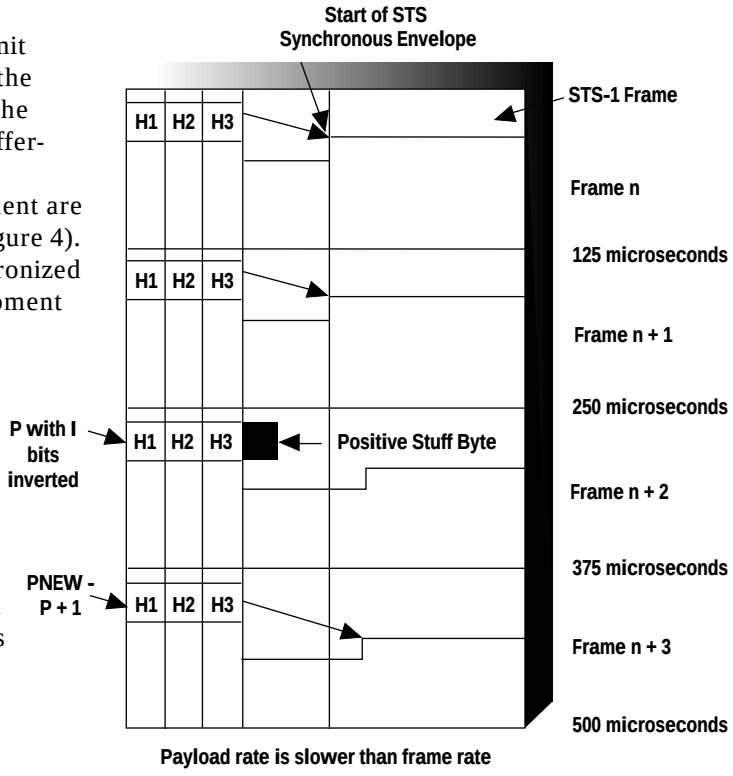

Figure 4. SONET pointer adjustment.

Telecommunications Synchronization

Most telecommunication administrations use the hierarchical source-receiver method to synchronize their E1/DS1 network. The master clock for a network is one or more primary reference sources (PRS). This clock reference is distributed through a network of receiver clocks (Figure 5).

A node with the most stable, robust clock is designated as a source node. The source node transmits a timing reference to one or more receiver nodes. Receiver nodes usually have equal or worse performance than the source node. The receiver node locks on to the timing reference of the source node and then passes the reference on to other receiver nodes. Timing is thereby distributed down a hierarchy of nodes.

Receiver nodes are usually designed to accept two or more references. One reference is active. All other alternate references are standby. In the case where the active reference is lost or is in error, the receiver node can switch references and lock to an alternate reference. Thus, each receiver node has access to timing from two or more sources. Most networks are engineered so that all receiver clocks are given two or more diverse references. In private networks, this may not be possible due to limited connectivity between nodes.

Clocks are placed into the hierarchy based upon performance levels. ANSI [2] designates performance levels as stratum levels: strata 1, 2, 3, 4E, and 4, in order of best performance to worst. ITU [3] designates four performance levels: primary reference source (PRS), transit node, local node, terminal or customer premises equipment (CPE) node. In addition, Bellcore [5] has defined a new level called stratum 3E, which is between ANSI stratum levels 2 and 3 in performance. Stratum 3E has not been adopted by any standards body.

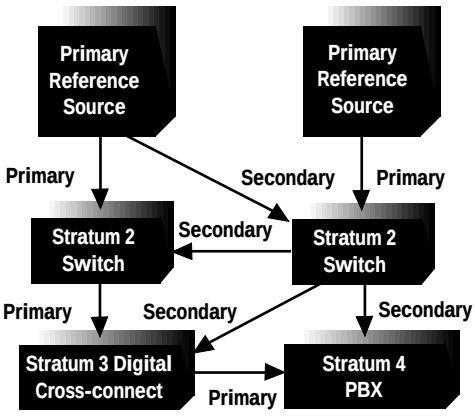

Figure 5. Hierarchical source-receiver operations.

Stratum 1 or primary reference sources are master nodes for a network. Stratum 2 or transit node clocks are typically found in toll switching and some digital cross-connect equipment. Stratum 3E is used in timing signal generators for use in networks with SDH or SONET. Local switching, most digital cross-connect systems, and some PBXs and T1 multiplexers have stratum 3 or local node clocks. Most T1 multiplexers, PBXs, channel banks, and echo cancellers incorporate Stratum 4 or CPE clocks. Further discussion of the functionality and role of receiver clocks can be found in [1].

Primary Reference Sources

A primary reference source (PRS) is a master clock for a network that is able to maintain a frequency accuracy of better than 1×10^{-11} [2, 4]. One class of PRS is a stratum 1 clock. A stratum 1 clock, by definition, is a free running clock [2]. It does not use a timing reference to derive or steer its timing. Stratum 1 clocks usually consist of an ensemble of Cesium atomic standards.

However, a PRS does not need to be implemented with primary atomic standards [2]. Other examples of PRS are Global Positioning System (GPS) and LORAN-C clocks. These systems use local rubidium or quartz oscillators that are steered by timing information obtained from GPS or LORAN-C. They are not considered stratum 1 since they are steered, but are classified as PRSs. These clocks are able to maintain an accuracy within a few parts in 10^{-13} to a few parts in 10^{-12}.

III. Synchronization Planning Concepts

A synchronization plan is the determination of the distribution of synchronization in a network. It involves the selection and location of a master clock or clocks, the distribution of primary and secondary timing, and the selection of the clocks and reference facilities. To achieve the best performance and most robustness from a synchronization network, several rules and procedures must be followed when developing a synchronization plan. Some of the most important rules are avoiding timing loops, maintaining a hierarchy, following the BITS concept, using the best facilities for synchronization reference transport, and minimizing the cascading of the timing reference.

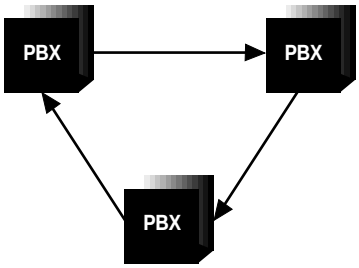

Figure 6. Timing loop.

Timing loops occur when a clock uses a timing reference that is traceable to itself (Figure 6). When such loops occur, the reference frequency becomes unstable. The clocks in a timing loop will swiftly begin to operate at the accuracy of the clock's pull-in range. This will result in the clock exhibiting performance many times worse than it does in free-run or holdover mode. Therefore, it is important that the flow of timing references in a network be designed such that timing loops cannot form under any circumstance. No combination of primary and/or secondary references should result in a timing loop. Timing loops can always be avoided in a properly planned network.

Maintaining a hierarchy is important to achieve the best possible performance in a network. Under ideal or stress conditions, passing timing from better to worse clocks will maximize performance. Synchronization will still be maintained in normal operation if timing is passed from a worse clock to a better clock. Only performance may suffer slightly, since a better clock is more immune to short-term network impairments and will accumulate less timing error. It is only in the case where an upstream clock enters holdover or free run that a non-hierarchy causes major problems. In this case, the poorer performing upstream clock in holdover may have a frequency accuracy worse than the downstream clock can lock to. The downstream clock will not remain locked and will also go into holdover. This results in multiple clocks being in holdover and excessive slips in the network.

Most administrations follow the Building Integrated Timing Supply (BITS) concept for synchronization distribution (Figure 7). In the BITS method, the best clock in an office is designated to receive timing from references outside the office. All other clocks in the office are timed from this clock. In many cases the BITS clock is a timing signal generator, whose sole purpose is for synchronization. Other administrations rely on clocks in switches or cross-connect systems for the BITS. The BITS clock should be the clock that is best performing in stress and holdover and is the most robust. By use of the BITS concept, the performance of the office will be dictated by the BITS clock, since only the BITS clock is subjected to stress on its timing reference.

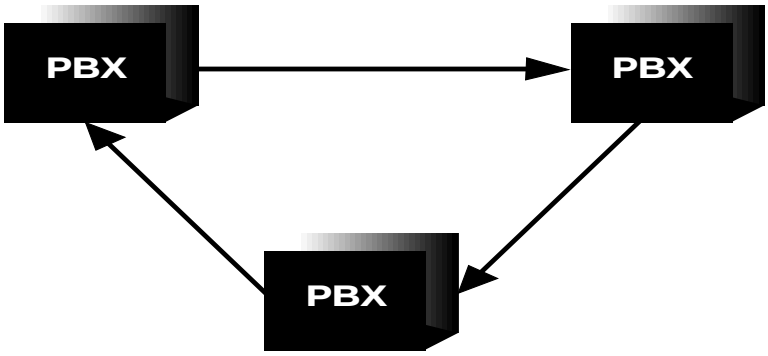

Figure 7. BITS with dedicated timing facilities.

Using the best facilities to transport a synchronization reference is required to minimize slips. The best facility may be defined as the reference with the fewest impairments. This refers to a reference that has the least average number of severely errored seconds (SES) [1] and that is free from excessive timing instabilities (jitter and wander). References that are payloads on SDH/SONET should not be used for timing, since they are subjected to pointer processing, which adds excessive wander and jitter to the reference. Similarly, references that are transmitted by ATM Constant Bit Rate services will exhibit large amounts of wander and should not be used for timing.

Cascading of timing references through a network should be minimized (Figure 8). Timing performance will always degrade as timing is passed from clock to clock. The more clocks and facilities in a synchronization chain, the greater the accumulated degradation will become, and the larger the frequency offset grows. Each facility will add impairments to which the clocks in the chain must react. Therefore, for best performance, synchronization chains should be kept short.

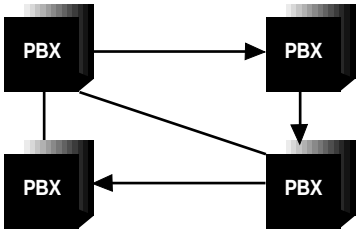

Figure 8.
Excessive cascading.

IV. Synchronization Planning Requirements

The synchronization plan for a network must meet several requirements, ranging from meeting performance objectives and satisfying service needs to being easy to maintain and administer.

Several performance objectives have been established by ITU, ETSI, and ANSI to control slip rates in carrier networks. ITU, ETSI, and ANSI allow the long-term frequency inaccuracy at the output of a digital system clock to be no worse than 1×10^{-11} [2, 3, 9]. Short-term requirements of 1 to 10 microseconds of time error in a day must also be met at the output of each network clock.

In private networks, ANSI requires that the first customer premises equipment (CPE) in the synchronization chain have no more than 4.8 milliseconds of time error per day. This corresponds to 40 slips per day, but it is only an interim requirement. In the next few years, this requirement is expected to change of 18 microseconds of daily time error.

Service requirements for synchronization depend on the application. ITU has established a slip rate threshold of one slip in every five hours for an “acceptable” end-to-end connection that will support the service needs of digital data, video, facsimile, and most encrypted services. In some networks, a tighter requirement of one slip per day is needed to support encryption. Signalling System 7 networks also typically require no more than 1 slip per day. All these service requirements will be achieved if the 1×10^{-11} long term frequency accuracy and 1 to 10 microsecond daily timing error requirements are met.

SDH and SONET services require good short-term stability. ANSI requires that the band-limited short-term noise at the output of any clock not exceed 100 nanoseconds. In addition, the band-limited short-term noise from a BITS clock should not exceed 17 nanoseconds. This implies that the network operate at a stratum 3E [5] or local clock performance levels.

V. Carrier Networks

Carrier networks require stringent synchronization planning if performance goals are to be achieved under normal operating conditions. A receiver clock normally operates with a frequency offset compared to the source clock to which it is locked [1]. This frequency offset accumulates in a chain of clocks. It is a goal of carrier synchronization planning to ensure that these accumulated frequency offsets do not exceed the required 1×10^{-11} frequency accuracy.

Since synchronization performance is dominated by receiver clock and facility performance, the major focus of synchronization planning for carrier networks lies in the determination of *timing distribution* and the *selection of clocks* and *facilities* used to time the network. The selection and determination of the number and locations of master clock or clocks for the network are largely based on performance goals and maintenance issues.

Carrier Network Synchronization Performance

The synchronization performance in a carrier network is characterized by three components: the accuracy of the master clock, the performance of the facilities distributing the reference, and the performance of the receiver clocks obtaining a reference over the facility [1].

The inaccuracies of the master clock usually contribute a small portion of the timing inaccuracies in a synchronization network. Primary reference sources (PRS) typically have long-term accuracies on the order of a few parts in 10^{-13} to a few parts in 10^{-12}. This performance is usually 10-100 times better than the performance of receiver clocks locked to the PRS.

Synchronization performance is dominated by a combination of the facility and receiver clock performance [1]. In normal operation, a receiver clock must lock to a source clock by extracting timing from a facility that has short disruptions or error bursts. The number of error burst events can range from an average of 1 to 100 events per day, depending on facility type, mileage, and other factors.

These constant degradations will adversely affect the distribution of the timing reference. The receiving clock will react to each error. It is allowed to move up to 1 microsecond in response to each error on its timing reference. Accumulation of facility errors and the resulting phase error in the receiving clock can result in the receiver clock operating with a frequency inaccuracy of a few parts in 10^{-12} to a few parts in 10^{-10}. Therefore, receiver clocks contribute a much larger portion of timing errors and slips in a network than the PRS will.

Primary Reference Sources

Almost all carriers with digital networks rely on primary reference sources (PRS) for timing since ITU recommends that networks operate with a long-term accuracy of 1×10^{-11} [3]. A PRS is placed in a network as shown in Figure 9. The PRS times all the equipment in the location in which it resides. This equipment, in turn, will time the rest of the network.

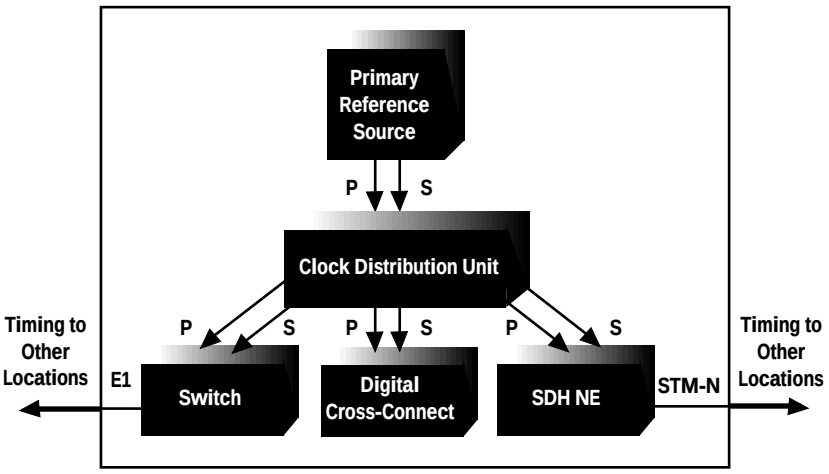

Figure 9 Primary reference clock configuration.

The slip rate contribution of a PRS is usually negligible. A network which derives timing from two PRS clocks will experience at most five slips per year, caused by the inaccuracy of the two clocks. This is negligible compared to the performance of receiver clocks. Receiver clocks typically operate with a daily performance that is 10 to 100 times worse than the PRS to which they are slaved. Therefore, it has been the trend of telecommunication network operators to rely more heavily on PRS clocks and to use multiple PRS clocks to time their network. This reduces the cascading of timing in the synchronization network.

The choice of PRS technology used by an administration depends largely on reliability, maintenance, and control. Performance is usually a secondary concern. LORAN-C or GPS technologies have been used extensively in North America. However, since GPS is controlled by the U.S. Department of Defense and LORAN-C is not global, many other administrations rely on Cesium clocks.

The locations in which the PRSs are used are determined by network topology. PRSs are usually placed in locations that will minimize the cascading of timing in the network. In this manner, the best performance can be achieved in the network. Additional sites that may require the use of PRSs are international switching locations. It is at these locations that one administration interfaces with another and all signals are transferred plesiochronously. It is important, therefore, to guarantee that these locations operate with the 1×10^{-11} frequency accuracy necessary for plesiochronous operation.

Interoffice Timing Distribution

The determination of the distribution of primary and secondary timing through a network depends on the network topology and performance requirements. Interoffice timing is configured such that timing loops are avoided, the hierarchy is maintained, cascading is minimized, and performance goals are met. Most administrations use traffic-bearing lines between offices to pass timing. Some rely on dedicated timing-only facilities between offices for improved maintenance, reliability, and performance.

Facilities with the best error performance, in terms of lowest number of daily severely errored seconds (SES) and least downtime, should be chosen to carry synchronization. Error rates typically correlate with the length of the facility. Therefore, short facilities are preferred. Satellite facilities are not used for timing distribution due to diurnal wander [1]. References that are carried as traffic in Constant Bit Rate ATM, SDH, or SONET are also not used to carry the reference due to excessive wander.

Most DS1/E1 references passed between locations are carried on facilities that use asynchronous multiplexing (e.g., DS3 multiplexing). These multiplexers utilize pulse stuffing methods (see Section II, Pulse Stuffing) to transmit the reference without retiming or changing the long-term frequency of the signal. The inclusion of asynchronous multiplexing in the reference signal will not significantly affect synchronization performance or planning as long as jitter levels caused by the multiplexing remain controlled.

The amount of reference cascading that can be allowed from the PRS to all other clocks in the network depends on the facility and BITS clock performances and the performance objectives of the network. The design objective for most networks is 1×10^{-11} long term frequency accuracy or 1 microsecond per day of timing inaccuracies (Section I). To achieve this level, BITS clocks must have rearrangement maximum time interval error (MTIE) performance of less than 1 microsecond, facilities can only have a few errors per week, and timing cannot be cascaded to more than two to four offices. If very good BITS clocks and facilities are used, more cascading can be allowed and a fewer number of PRSs are required in the network.

Intraoffice Timing Distribution

The BITS configuration is the recommended method for intraoffice timing (see Figure 7 on page 9). By using a BITS, the best clock controls the office, cascading is minimized, and administration is easier. In the BITS method, all equipment in the location receives two diverse references from the BITS in a star arrangement.

The stratum level required in a BITS clock is largely determined by performance requirements and the size of office. Stratum 2 and transit clocks are typically used in large toll offices, whereas stratum 3 or local clocks are used in smaller locations. If there is SONET or SDH equipment in the location, it is recommended that the BITS clock be at least a stratum 3E or local clock, respectively [5]. This is to minimize the number of pointer adjustment events occurring on traffic through the SDH/SONET system.

Determination of which clock is best for a given stratum level is based on performance and maintenance issues. The most important performance parameter distinguishing clocks at the same stratum level is the MTIE during rearrangement [1]. This performance parameter will have the greatest impact on daily performance of any function of the BITS clock.

Timing the BITS Clock

The BITS clock receives two or more references from other locations. If dedicated facilities are used to time the BITS clock, the facilities will terminate directly on the BITS (see Figure 7 on page 9). When traffic-bearing facilities are used, the reference facility that is chosen typically does not terminate on the BITS clock. In these cases, a device called a bridging repeater is used (Figure 10). A bridging repeater is an in-line device that taps onto any DS1/E1 signal and provides a copy of that signal. In this manner, any traffic-bearing line coming into an office can be used as a timing reference for the BITS clock.

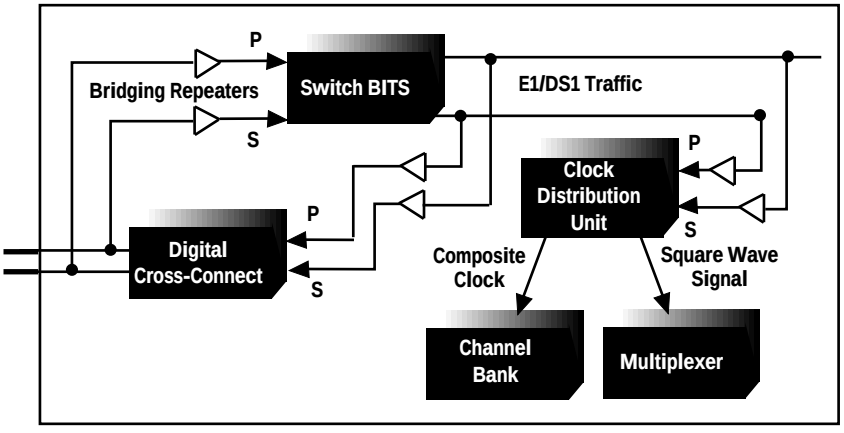

Figure 10.
Switch BITS clock.

In order to receive timing not terminated on the clock, the BITS clock also requires external timing capabilities. External timing is the feature of having ports on the device dedicated for synchronization only. Some equipment, however, can only extract timing from traffic that terminates on the equipment. If such equipment is chosen for the BITS and the reference line does not terminate on it, the carrier must dedicate two (or more) traffic ports to be used for synchronization only.

An important factor in supplying timing to the BITS clock must be that diversity is maintained among the references. Diversity must be achieved at all levels. The timing source should be diverse, coming from a different location and different equipment, over diverse facilities. In addition, power to all devices in the synchronization path, including facility multiplexers and bridging repeaters, should be diverse.

Timing Distribution from the BITS Clock

The BITS clock is used to provide synchronization to all equipment in its location. There are several methods used for intraoffice timing distribution: dedicated DS1 and E1 synchronization lines, synchronous clock insertion units, composite clock lines, and square and sine wave signals.

DS1 and E1 signals are typically used to time digital switches and cross-connect systems in an office. If a timing signal generator (TSG) is used as the BITS, the TSG will supply these signals directly (Figure 11). If a digital switch or cross-connect system is used as the BITS clock, the device will typically only transmit traffic and not synchronization signals. Therefore, with a switch or cross-connect BITS, a bridging repeater or a clock distribution unit (Figure 10) is used to supply DS1 and/or E1 timing signals.

Bridging repeaters are tapped into any outgoing DS1/E1 traffic-bearing line from the switch or cross-connect BITS clock. These bridging repeaters can now supply timing (traceable to the BITS clock) to other clocks in the office.

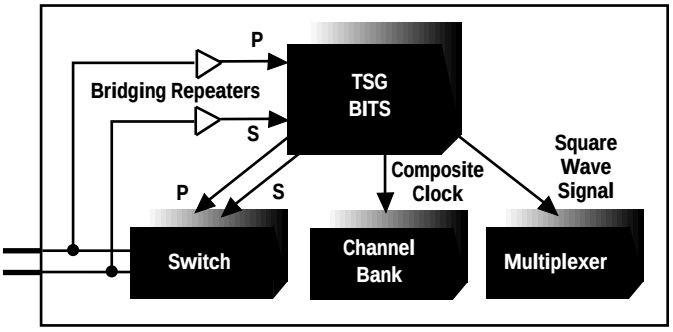

Figure 11. TSG BITS clock.

Clock distribution units (CDU) are devices that accept a DS1/E1 reference and supply multiple references. They essentially act like a multiplicative device giving multiple references out for one incoming reference. A clock distribution unit is distinguished from a TSG in that the CDU does not include a clock and does not retime the line. It has no reference switching or holdover functions that are normally associated with a clock. If the input line to a CDU is lost, the CDU will cut off signals to all outgoing lines.

The DS1/E1 BITS reference from the TSG, bridging repeater, or CDU is connected to the external timing input of all equipment in the location. The equipment which does not have external timing capability can receive timing directly from the BITS clock by either dedicating traffic ports for synchronization use only or by using a synchronous clock insertion unit (SCIU) (Figure 12). An SCIU is a device whose only function is to reclock a DS1/E1 line that is passed through it. Other than reclocking, the SCIU does not affect the line being sent through it. With the use of the SCIU, BITS clocking can be injected on traffic-bearing lines and sent to equipment that does not have external timing. The advantage of the SCIU is that a star arrangement can be maintained without requiring the use of extra DS1/E1 ports in the receiving equipment.

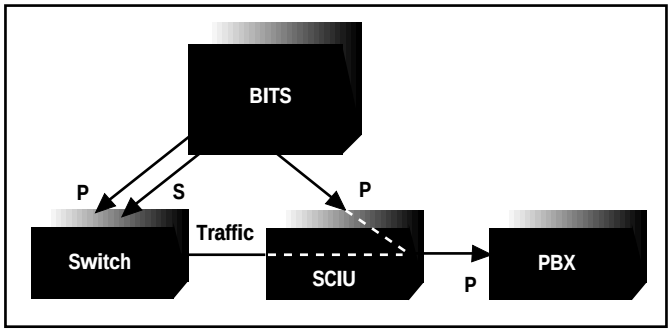

Figure 12. Synchronous Clock Insertion Unit.

In some equipment, the external timing input does not accept an external DS1 or E1 signal, but rather a 2.048 MHz, 1.544 MHz, or 8 KHz square or sine wave timing signal. For this equipment, TSGs and CDUs will often have square and sine wave timing signal options. These can be used to directly time the equipment. Many administrations, however, do not use this option and will either time such equipment by an SCIU, or looped-time it [1] from other equipment in the location.

A composite clock is another means commonly used to time equipment in a location. A composite clock signal is used to synchronize equipment that has DS0 interfaces, such as channel banks with DS0 dataports and DDS equipment. The composite clock signal is a 64 KHz bipolar square wave with an 8 KHz signal riding on it in the form of a bipolar violation every 8 bits. Most TSG and CDUs will provide composite clock signals (Figures 10 and 11). Receiving equipment that uses composite clock signals requires only one timing reference. It should be noted that not all networks require composite clock signals.

Monitoring and Verification

A recent trend in telecommunication synchronization is the use of monitoring systems to verify synchronization performance [6]. The timing performance of an office can be verified by comparing the timing of a DS1 or E1 line coming from that office with the timing from a known, highly-accurate reference (Figure 13). Monitoring can be done real-time and continuously by using a bridging repeater to tap into the DS1 line to be monitored and continuously measuring the line relative to a primary reference source (PRS).

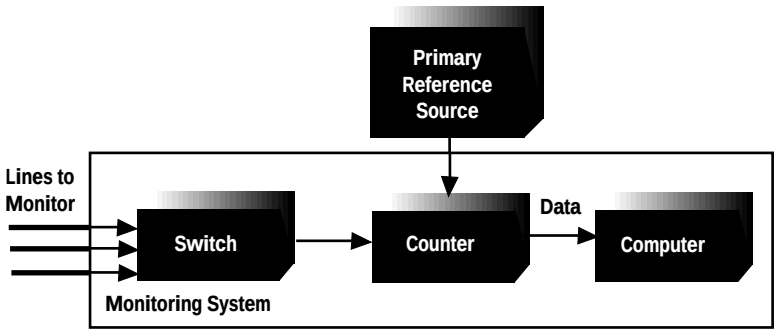

Figure 13. Synchronization Monitoring System.

Verification is needed to detect and resolve timing degradations before they impact service. There are numerous sources of timing degradations, such as maintenance activities, circuit re-provisioning activity, clock diagnostics, and excessive facility errors [6]. These degradations are not easy to detect or diagnose using standard alarm mechanisms. Monitoring allows for instant detection and simplified diagnostics of synchronization problems.

SONET/SDH

SDH and SONET use a pointer mechanism (see section II, Pointers, on page 5) to identify the beginning of frames in their payload. If the payload timing differs from the SDH/SONET network element, or if the timing of two SDH/SONET network elements differs, adjustments are made in the pointers. Pointer adjustments cause significant amounts of jitter and wander. Therefore, ANSI [2] recommends that timing is never passed as payload through an SDH/SONET facility. It recommends instead that timing is extracted from the optical signal (Figure 14). In this case, the timing is derived from the previous SDH/SONET network element (NE) in the facility.

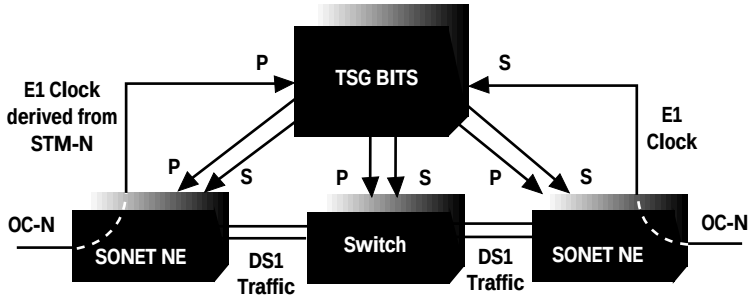

Figure 14. Timing distribution using SONET lines.

SDH and SONET also place further restrictions on the synchronization plan since BITS clocks in offices with SDH or SONET equipment should have at least a stratum 3E or local clock. This is to minimize the number of pointer adjustment events occurring on traffic through the SDH/SONET system.

Further discussion on the impact of SDH and SONET to synchronization can be found in [7].

VI. Private Networks

Synchronization planning for digital private networks is extremely difficult since the private network topology is typically complex and unconstrained. The widespread use of stratum 4 clocks in these networks can lead to severe performance degradations and force excessive cascading of the timing reference. Private networks are also in a multivendor, multicarrier environment which makes synchronization planning complex. Proper planning requires the knowledge of the entire digital private network. All digital equipment and digital services must be included in the plan.

An additional complexity with private networks synchronization planning versus carrier network planning is that most reprovisioning in the private network affects the synchronization plan. This is because of the limited connectivity in a private network. A new plan is needed if any digital service, facility, or equipment is added, deleted, or changed in a private network. This is usually not the case in carrier networks.

Private Network Synchronization Performance

The majority of private networks rely on stratum 4 CPE clocks for their timing. Since stratum 4 CPE clocks perform 100-1000 times worse than stratum 4E or better clocks, private network synchronization performance is dominated by the performance of stratum 4 clocks.

Under stressed conditions, stratum 4 CPE clocks perform very differently than other network clocks. When a stratum 4 clock experiences a short interruption, it will declare the reference unusable and will switch its reference to a backup timing source, either another timing reference or its internal oscillator. During the reference switch, the clock will typically produce a large, fast phase hit of 10 to 1000 microseconds. This phase hit is often large enough to cause multiple slips and occurs on all outgoing lines of the CPE.

Downstream clocks are unable to remain locked to a reference with such a phase hit. To the downstream device, the phase hit is indistinguishable from a facility error. As a result, the downstream clock will switch its reference, cause another phase hit, and the error event propagates. Therefore, one error on a facility at the top of the synchronization chain can cause all lines and nodes in the synchronization chain to have errors (Figure 15).

Since transmission facilities carrying the timing reference can have from 1 to 100 error bursts per day, the performance of private networks using stratum 4 clocks is typically poor. It can be 1,000 times worse in performance than is seen in public networks, operating at an effective long-term frequency accuracy of 1×10^{-9} to 1×10^{-7}. Slip performance of dozens of slips per day per CPE is not unusual.

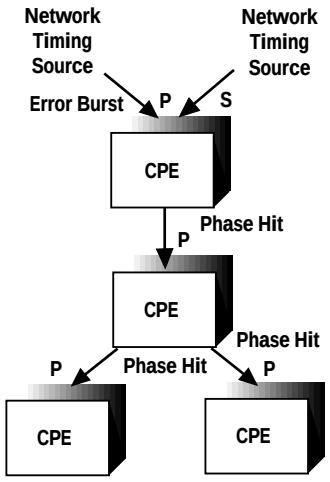

Figure 15. Cascading errors in private networks.

Synchronization Sources

Private networks typically do not own and operate their own PRSs, but rather rely on the service-provider for timing. Many services provided by the carrier has timing that is traceable to a PRS. The private network can receive timing from these services.

It must be noted that not all services provide timing. The private network operator should check with the service provider to see if timing is provided. In general, in North America, switched services are timed, whereas point-to-point services may or may not be timed.
In Europe, both switched and point-to-point services usually have timing.

To optimize synchronization, the private network should receive timing from as many PRS-traceable sources as possible, even if the sources come from different carriers. This will provide the best performance in the private network. In normal operation, the frequency accuracy of carrier network equipment is typically 100-1000 times better than that of a CPE [6]. Therefore, the synchronization performance of a CPE will improve if it receives timing directly from a carrier source, as opposed to cascaded timing from another CPE. The use of multiple PRS-traceable timing sources improves performance, minimizes cascading of timing, and increases the diversity of timing sources in the network.

If the private network does not have any service that provides PRS traceable timing from the carrier, the private network must designate a master clock for the network (Figure 16). In this case, the private network is a digital island and does not interface digitally with any PRS traceable equipment. Therefore, the private network does not need to be timed from a PRS. The designated master clock is the clock with the best free-run performance. The clock should also be centrally located in the network so that cascading of timing can be minimized. This master clock, usually a digital Private Branch Exchange (PBX) or multiplexer, is set to free-run. All equipment in the network obtains timing traceable to the master clock.

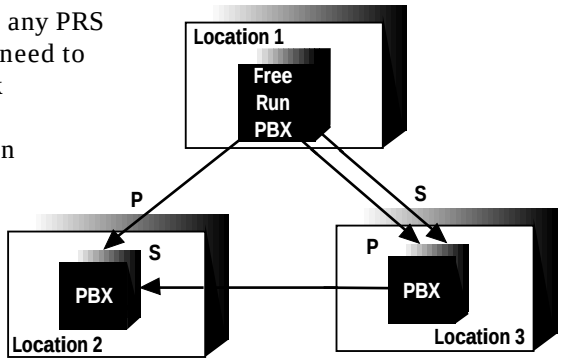

Figure 16. Location 1 PBX is Network Master Clock.

The hazard of operating a private network traceable to a clock that is not a PRS is when new services are added to the network. A new digital, PRS-traceable service can be added to the network later. The synchronization distribution must be changed so that the private network receives timing from the new service. If a new synchronization plan is not developed and master timing for the network remains as a free-running CPE, excessive slips will appear and make the new service unusable.

Interoffice Timing Distribution

Timing is passes between private network locations when a location is connected to the private network by point-to-point services that do not have carrier timing. This is typical in data networks. The rules for determining how timing is passed between private network locations is similar to carrier network rules: use the best (typically, shorter) facilities, minimize cascading, and avoid timing loops. Minimization of cascading is especially important in private networks since CPE cascade phase hits throughout a network. The shorter the synchronization chains are, the less stratum 4 CPE equipment is impacted.

The three major difficulties in interoffice timing in private networks are lack of secondaries, non-hierarchical situations, and diversity. Private networks typically have limited connectivity. Each location is connected to only a few other locations. Sometimes, it is impossible to provide a location with a secondary without forming a timing loop (Figure 17). In this situation, it is better to configure the network without a secondary than it is to run the risk of forming a timing loop. The performance of a CPE in a timing loop is typically 10-100 times worse than it is in free-run or holdover.

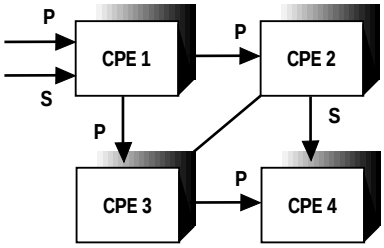

Figure 17. Either CPE 2 or CPE 3 cannot have secondary.

Non-hierarchical situations also arise due to lack of connectivity (Figure 18). Often, they are unavoidable. As discussed in Section III, the network will operate with non-hierarchical situations. These situations can be avoided by introducing a TSG in the timing source location.

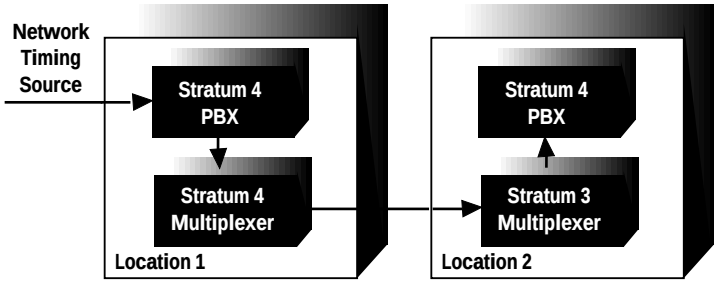

Figure 18. Location 2 Multiplexer has non-hierarchical timing.

Ideally, primary and secondary sources should be diverse, especially since most CPEs do not incorporate holdover in case of loss of all timing references. However, in private network diverse references may not always be possible. A location may be connected to only one other location. In many cases, access of private network service providers is not diverse. Also, in North America, having service from multiple carriers does not ensure diversity, since one carrier may lease lines from another.

Intraoffice Timing Distribution

In private networks, when a location relies on a CPE for timing, as opposed to a TSG, the use of the BITS concept is often infeasible or undesirable (Figure 19). Most CPEs do not have external timing options. Therefore, in order to use the CPE as a BITS, two dedicated DS1 ports (for synchronization uses only) and two bridging repeaters are required. This is usually more expensive than the cost of a TSG. In addition, if the CPE is not major equipment (such as a PBX or a multiplexer), the CPE is typically reprovisioned often and may not make a reliable timing source.

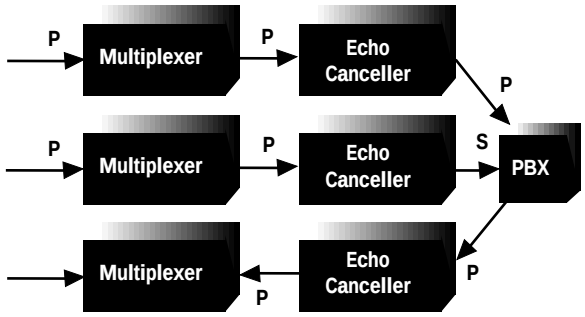

Figure 19. No BITS in private Network.

In situations where a BITS clock is feasible, the private network should use a BITS that has a stratum 4E or better clock, if available. If the private network is to meet the future ANSI requirement of no more than 18 microseconds of daily timing error, a stratum 4E or better BITS clock is required. Stratum 4 BITS clocks typically have daily timing errors that range from hundreds of microseconds to tens of milliseconds.

Dynamically Changing Synchronization Plans

Several CPE manufacturers incorporate a proprietary, dynamically-changing synchronization plan feature in their equipment. With this feature, the synchronization distribution continually changes among a network of equipment made by the manufacturer. One or more network timing sources are designated for the network. From these sources, the CPE automatically determines how to pass timing through the network, with the goal of minimizing the cascading of timing (Figure 20A). If a CPE loses its timing reference (Figure 20B), the entire synchronization distribution in the network will change to resupply all CPEs with a timing source with minimum cascading from the network reference.

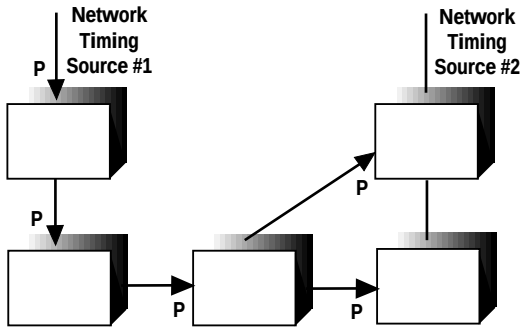

Figure 20A. Dynamic Synchronization Plan: Network timed from network timing Source #1.

In most cases, it is preferable for the private network to avoid the use of dynamic synchronization plans. Such a plan will lead to an excessive number of reference switching events. Since most CPEs with this feature have stratum 4 clocks, excessive reference switching causes large numbers of error bursts and very poor performance. In addition, the use of a dynamic plan does not allow the private network to follow the BITS clock concept and makes the network more difficult to administer.

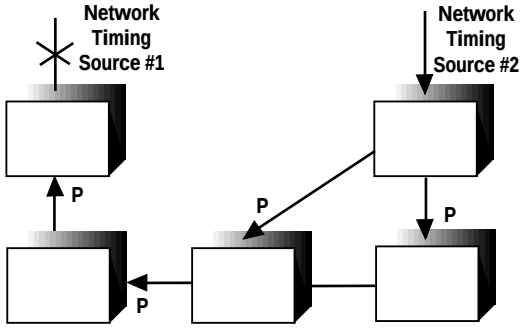

Figure 20B. Dynamic Synchronization Plan: Network timing source #1 fails.

SDH and SONET

As carriers introduce SDH and SONET into their networks, many private network services will be provisioned as payload on SDH or SONET systems. In these situations, all services for a private network location may be subjected to SDH/SONET pointer adjustments and the associated jitter and wander (Figure 21). Typically, the carrier's SDH or SONET equipment will not be on the private network operator's premises and, therefore, that operator will not have access to the SDH/SONET timing signal that is derived from the optical carrier. The private network operator must rely on the SDH/SONET traffic signal for timing. References passed as payload through SDH/SONET can have significant amounts of wander. A DS-1 or E1 signal, mapped and transported though SDH/SONET, can experience tens of microseconds of wander per day [8]. This situation is currently under study in standards bodies and affected private network operators are handled on a case-by-case basis by the service provider.

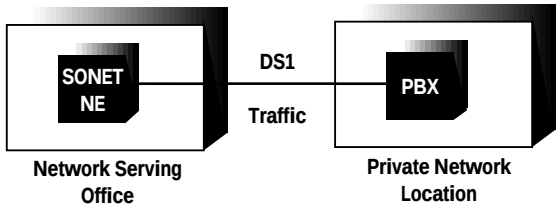

Figure 21. Private network service provided by SONET.

VII. Conclusions

Synchronization planning for telecommunication networks has been presented. Stringent planning must be done for all networks if performance objectives and service needs are to be met. In carrier networks, the major focus of synchronization planning for carrier networks lies in the determination of timing distribution and the selection of clocks and facilities used to time the network. Careful attention must be made to the selection of BITS clocks and reference facilities, and to the minimization of reference cascading. In private networks, the major goal of synchronization planning is to reduce errors caused and propagated by poor CPE clocks. This requires limited use of stratum 4 CPE clocks, limited cascading, use of as many carrier timing sources as possible, and the use of BITS architectures.

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[9] European Telecommunication Standards, "The Control of Jitter and Wander Within Synchronization Networks," Draft ETS DE/TM-3017.

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